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PCI Express System Architecture

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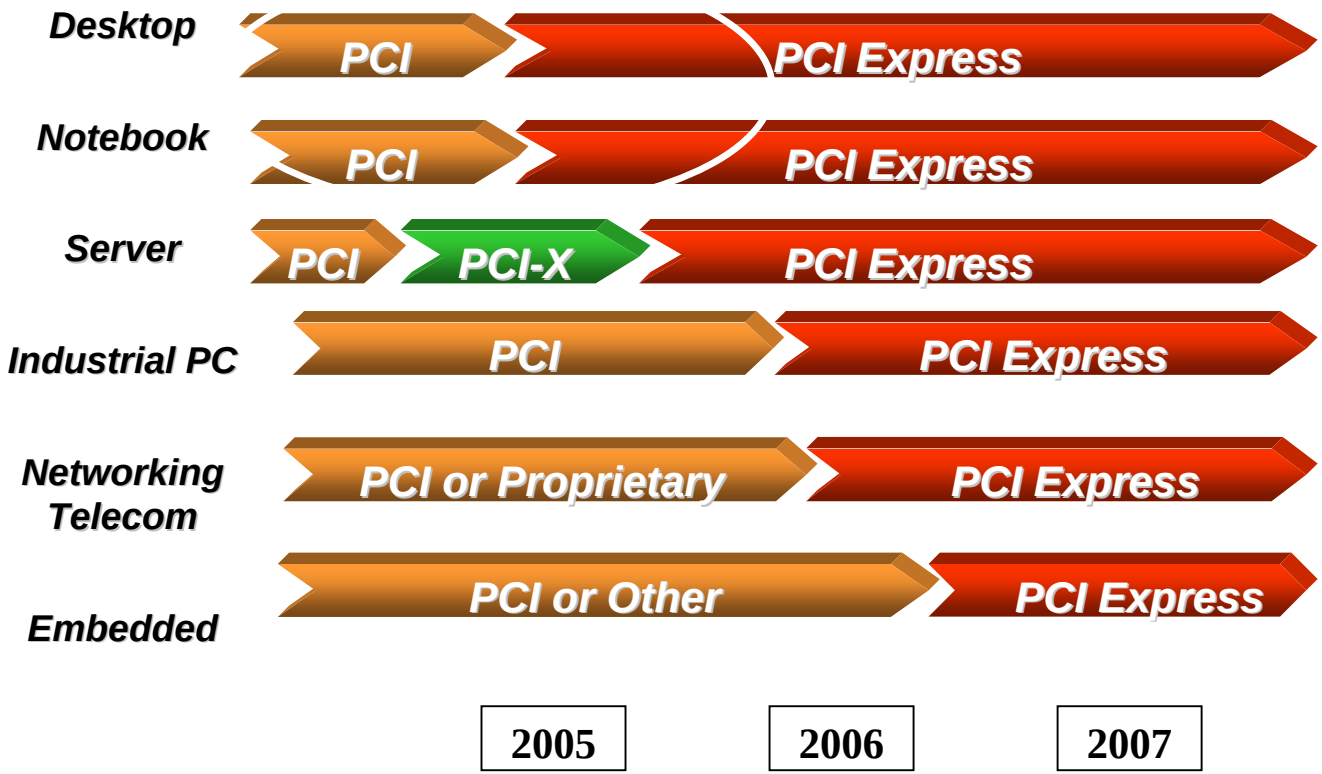
Agenda

- Basic Overview
- Features
- Device Layers & Packets
- Link Initialization & Training

Technology Shift to PCI Express



– All major markets are transitioning to PCI Express
  - Driven by new Intel chipset rollout, first market segments to transition are PC and Notebook

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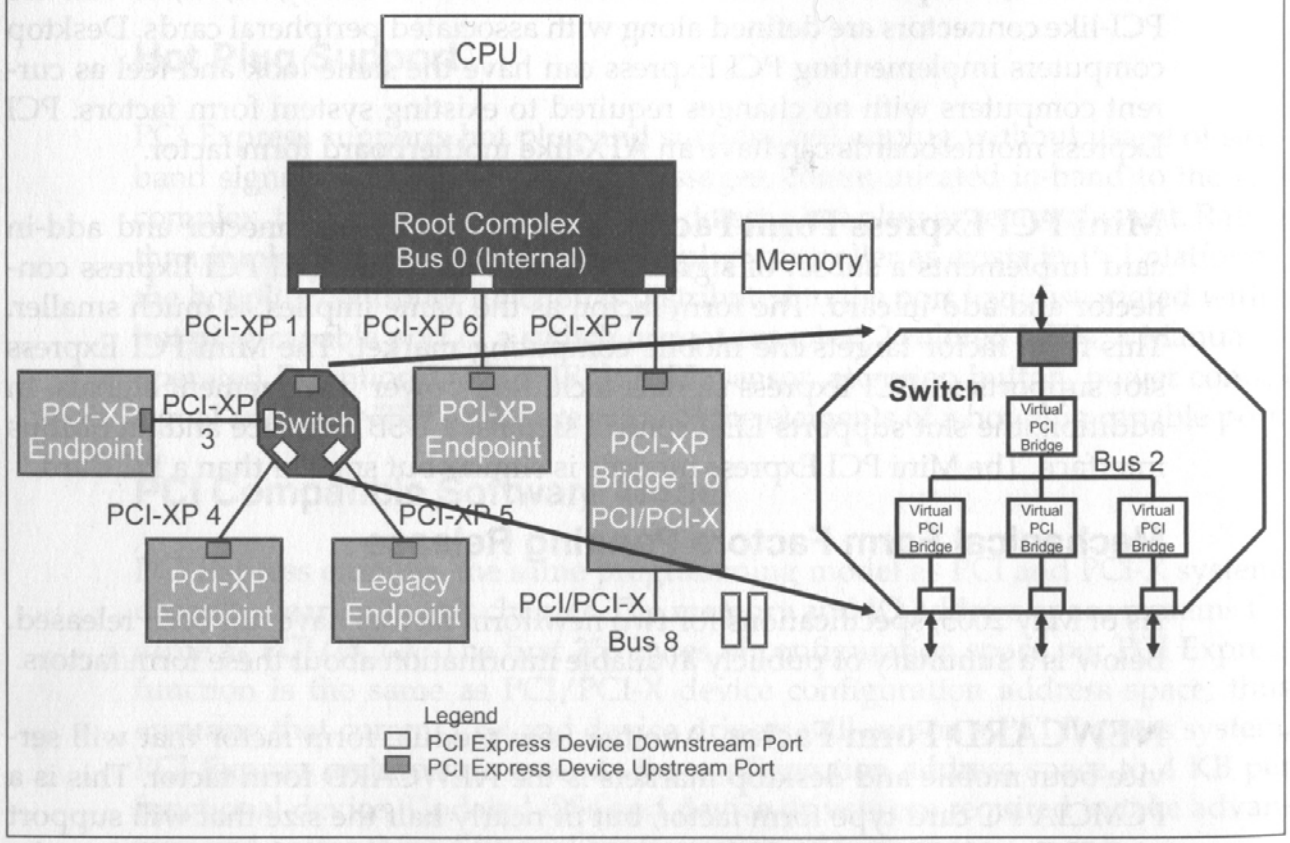
PCI Express Topology

Upstream port, Downstream port

Figure 1-22: PCI Express Topology



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Physical Layer PCI v.s PCI-Express

- PCI uses a shared parallel bus
  - Bandwidth shared between devices on the bus
  - Only one device may own the bus at any time
  - Large number of parallel signals
  - Wait states may be added by Initiator or Target
- PCI-Express uses a serial point to point interconnect
  - Full bandwidth dedicated to that link
  - No need for arbitration
  - Low number of signals
  - No wait states

Performance – PCI v.s PCI Express

PCI /PCI-X Bus	32bit 33Mhz	32bit 66Mhz	64bit 66Mhz	64bit 133Mhz
Bandwidth (GBytes/s)	0.132	0.264	0.528	1.064

- Bandwidth(GB) = Frequency(Mhz) x bit(Bytes)

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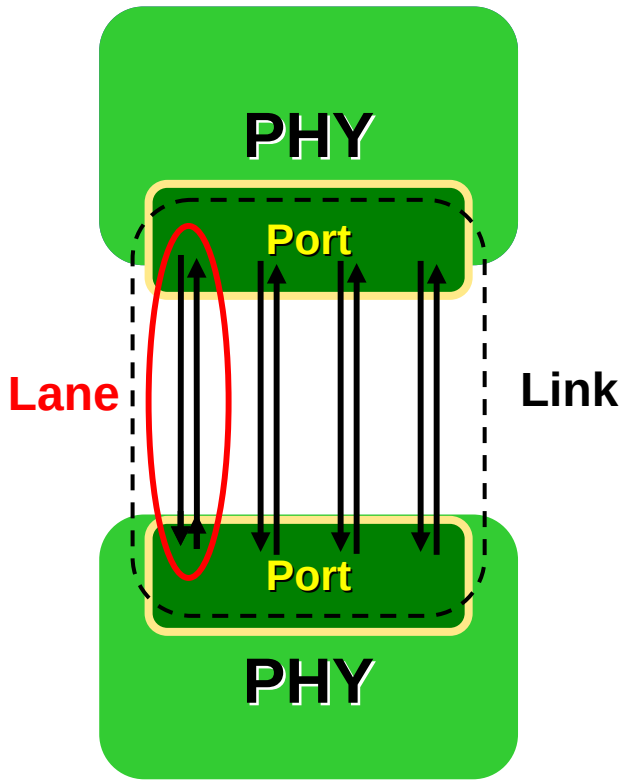
PCI Express Throughput

PCI Express Link Width(Lanes)	x1	x2	x4	x8	x12	x16	x32
Bandwidth (GBytes/s)	0.5	1	2	4	6	8	16

- 2.5Gbits/sec/lane/direction transfer rate
- Direction-Transmitter and Receiver(full duplex)
- Divide by 10-bits per Byte (8b/10b encoding)
  - Embedded Clock and Error Detection
- Multiply by number of lanes

Key Definitions

- Port
  - A group of transmitters and receivers located on the same chip that define a link
- Lane
  - A set of differential signal pairs, one pair for transmission and one pair for reception
- Link
  - A dual-simplex communications path between two components
  - A xN link is composed of N lanes



Example: 4 Lanes

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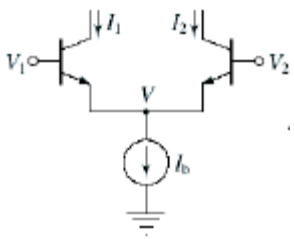
Features

- Point to point
- low voltage differential signaling
- Lane reversal and polarity inversion
- Speed, lane width, lane reversal and polarity negotiation at initialization
- Packet based transaction(Serial interconnect Technology)
- Flow control
- Transaction Layer Packet acknowledgements (Ack/Nak)
- Support VCs, TCs

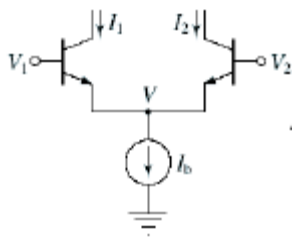
Low Voltage Differential Signaling

D+ D-

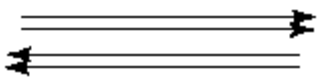


A Differential Pair (Transmitter)

D+ D-



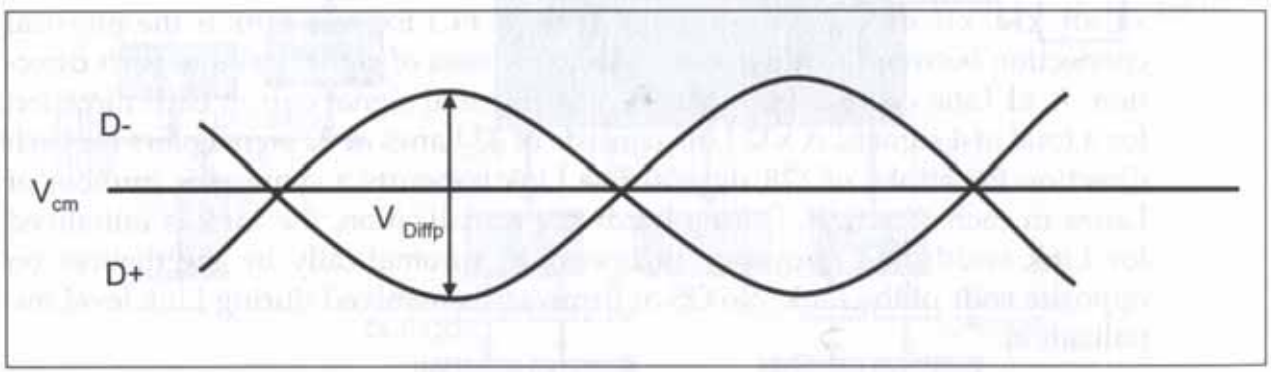
A Differential Pair (Receiver)



A Differential Pair In each direction = one Lane

This is an x1 Link
There are four signals

Figure 1-21: PCI Express Differential Signal



$V_{DIFFP-P}$:

800mV~1200mV

Vcm DC: 0~3.6V

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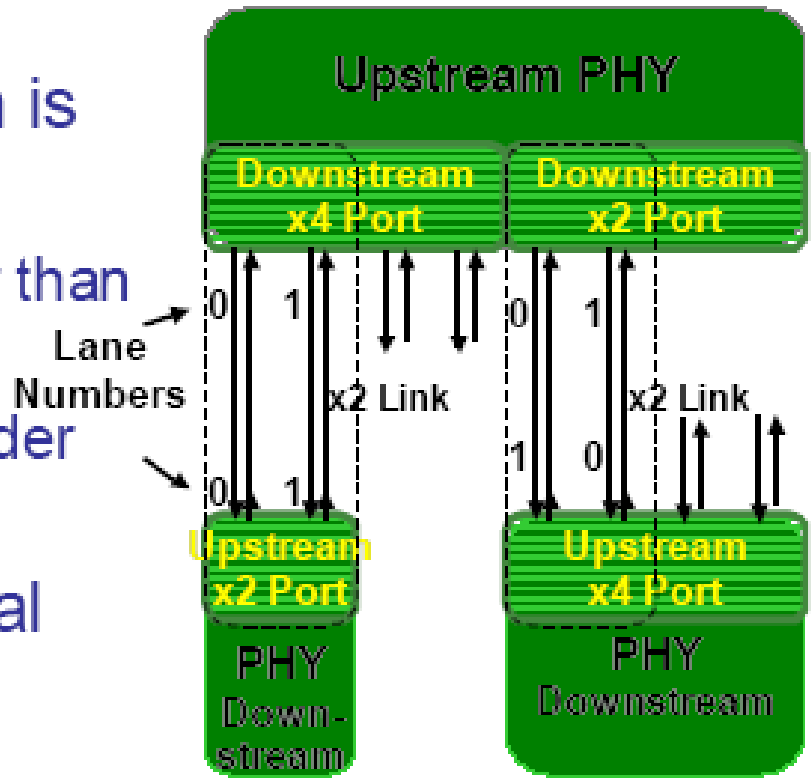
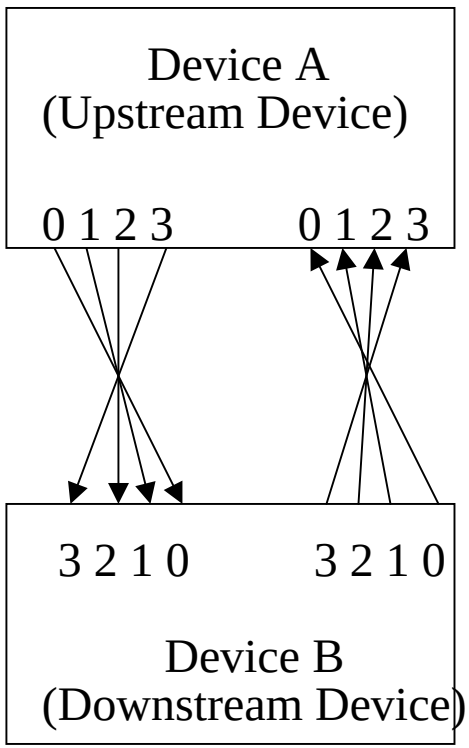
Link Configuration

- Configuring Link Width is Flexible
  - Upstream can be wider than downstream
  - Downstream can be wider than upstream
- Lane Ordering/Reversal
  - Lane ordering can be swapped within a link

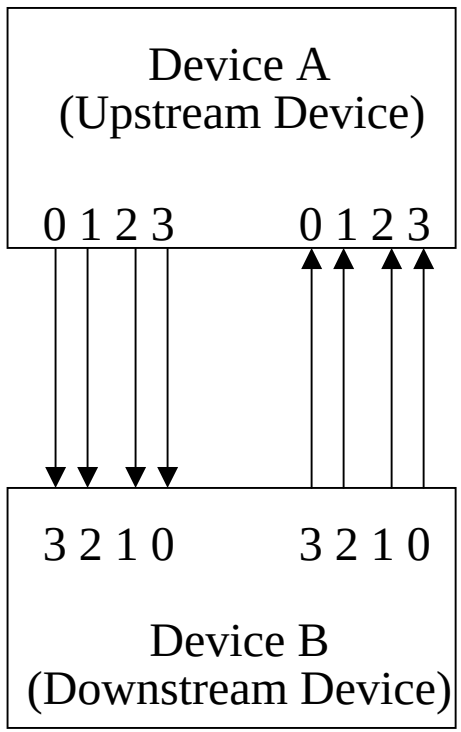


Lane Reversal

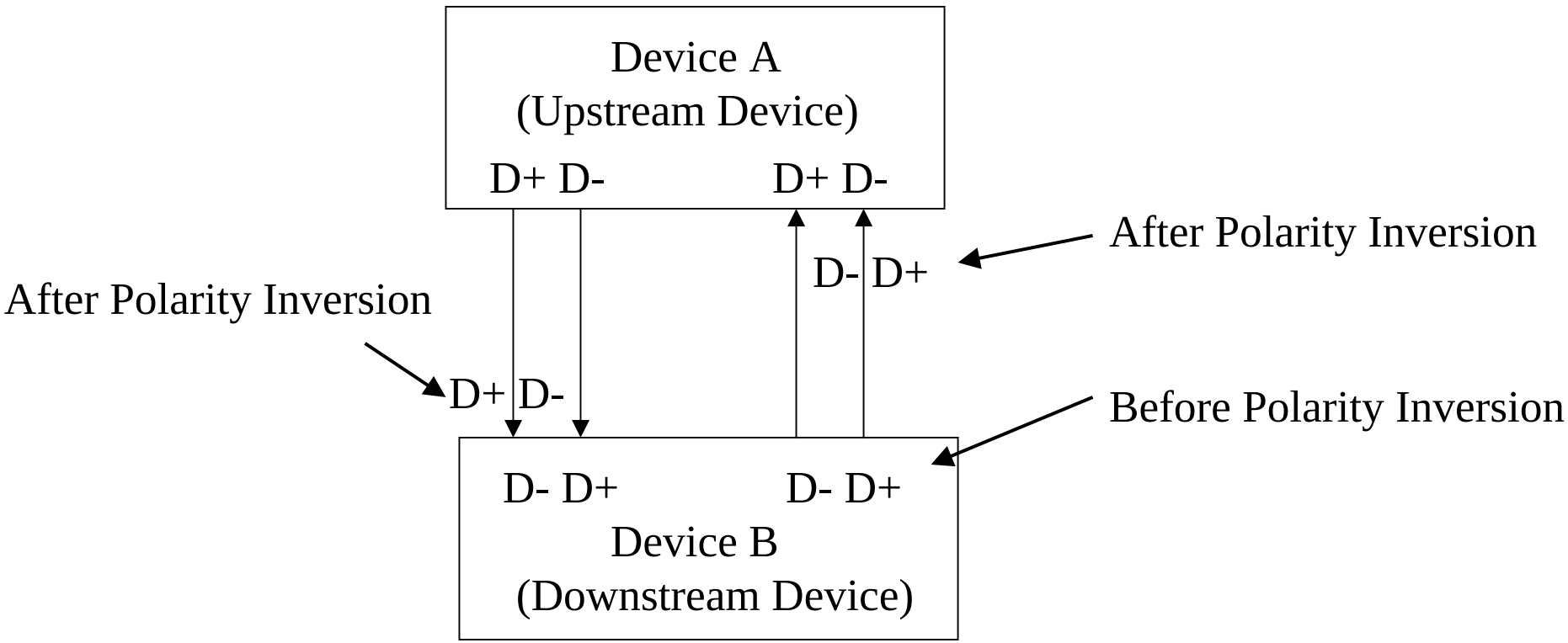
Neither device A nor B supports Lane Reversal



Device B supports Lane Reversal



Polarity Inversion



- **lane reversal and polarity negotiation at initialization**

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The Protocol Layers

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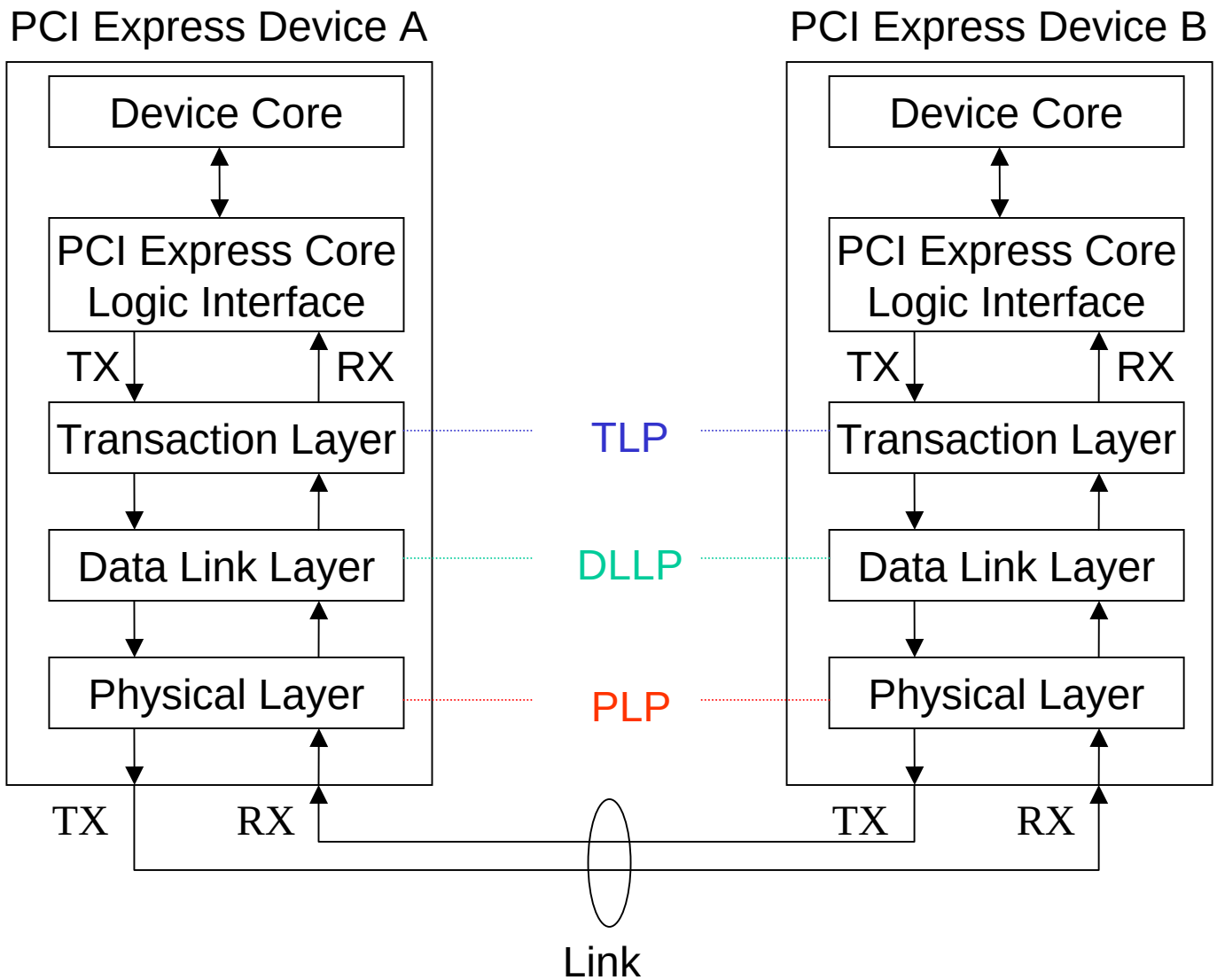
Device Layers



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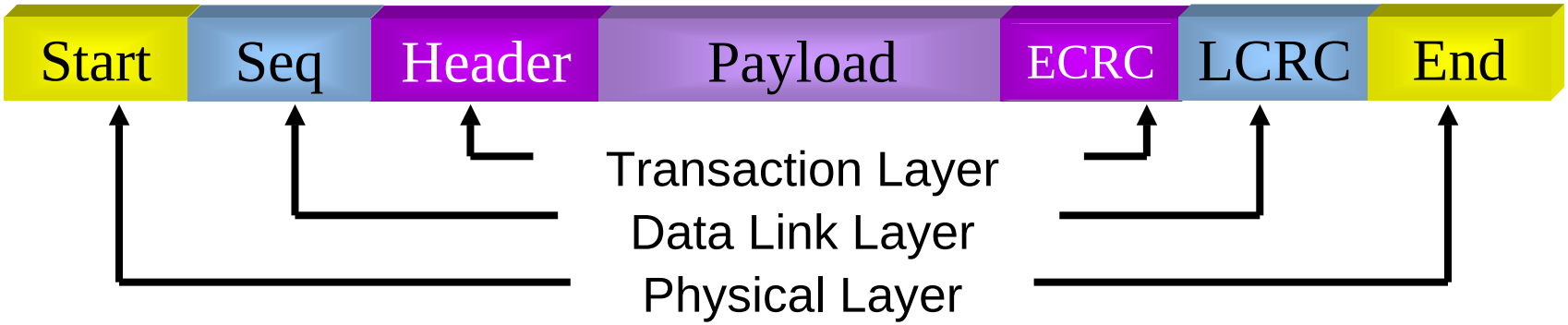
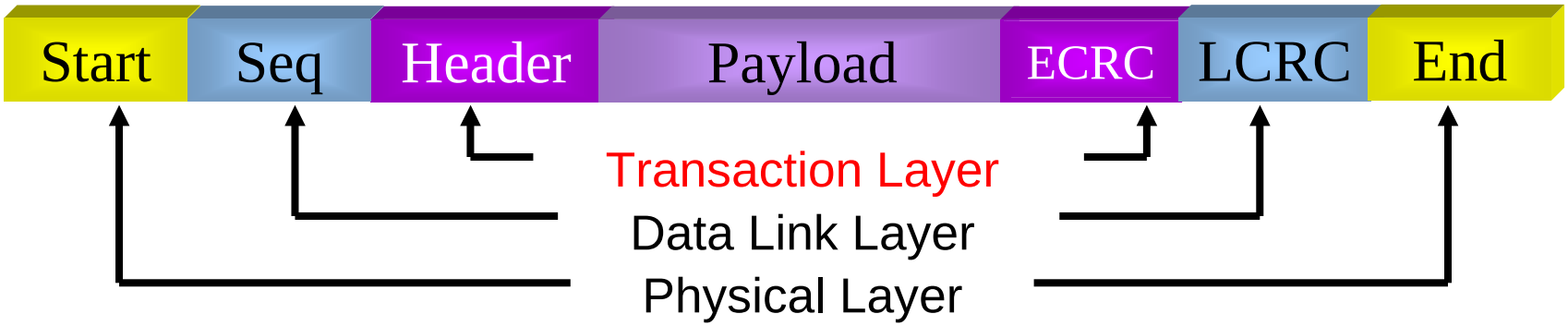
PCI Express Layers



- Packets are transmitted serially
- Credit based Flow Control
  - Each device transmits periodic flow control packets to inform transmitter of buffer space
  - Ensures that receiving device has buffer space for the packet

Transaction Layer



- Responsible for;
  - Storing negotiated and programmed configuration information
  - Managing link flow control
  - Enforcing ordering and Quality of Service(QoS)
  - Power management control/status
- Header

  Information may include;
  - Address/Routing
  - Data transfer Length
  - Transaction descriptor
- End to End CRC checking provides additional security(Optional)

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QoS General Information

- ACK/NAK ensure correct delivery of data
- Replay Timer allows Retry Buffer to be re-sent
- Can re-train the link in the event of catastrophic failure
  - Only one or some of the lanes may be corrupted
  - Retraining may allow fall back to lower bandwidth system.

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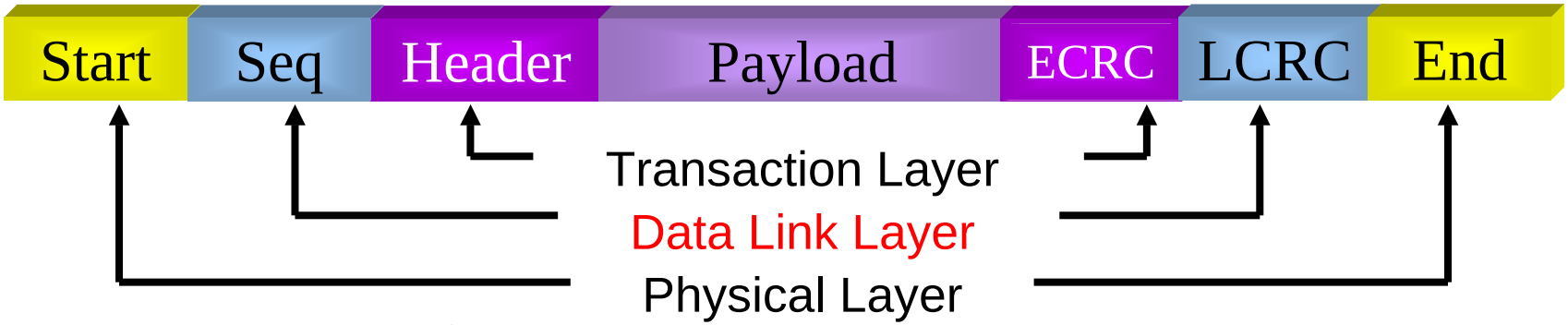
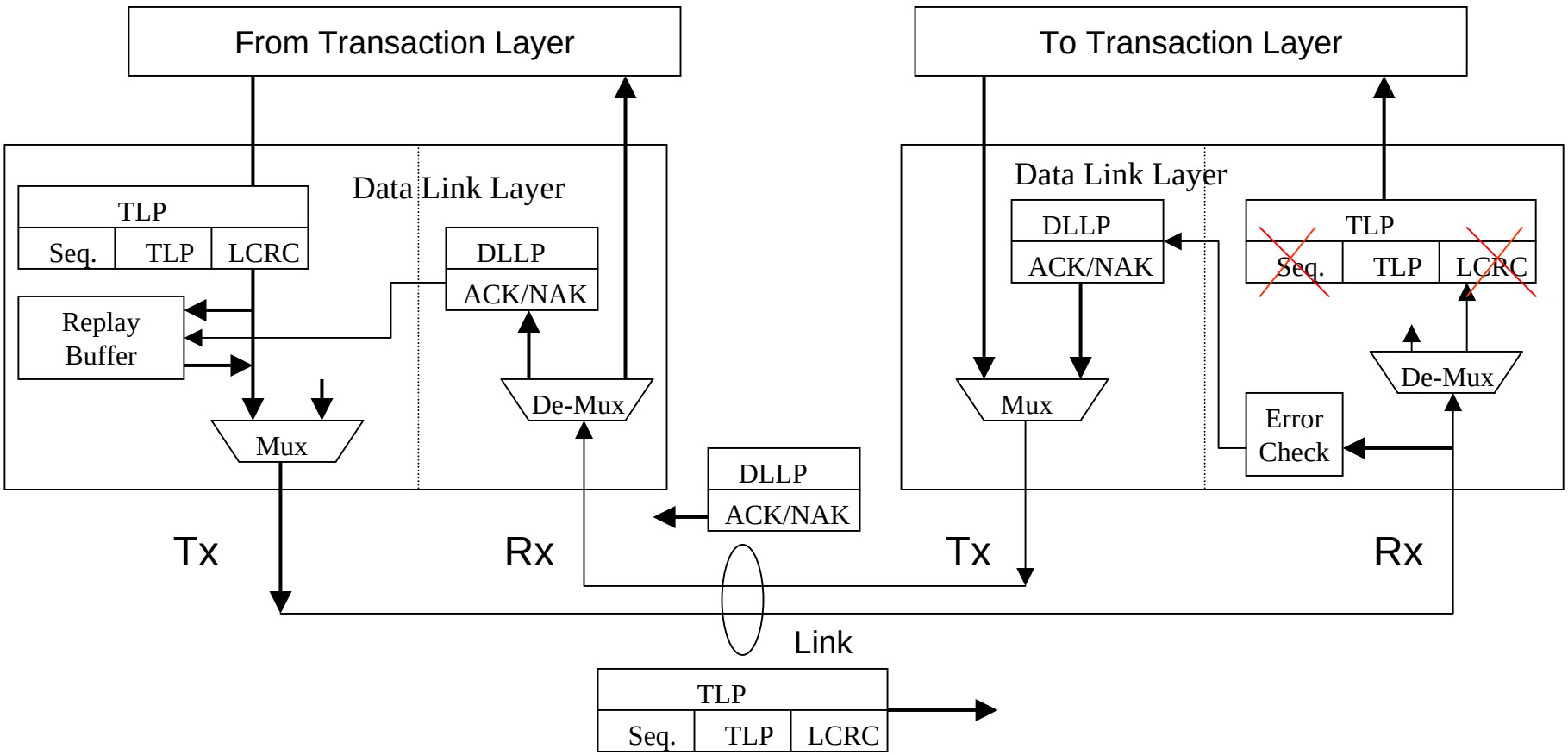
Data Link Layer Packets



- Responsible for;
  - Integrity of TLP's
    - Link-level error detection and re-transmission of bad TLP's
  - Initialization and updates of credit based flow control mechanism
- Classes of DLLPs
  - Transaction Layer Packet acknowledgements (Ack/Nak)
  - Power management
  - Flow Control (Flow Control packets)

ACK/NAK Protocol

- "Reliable" transport of TLPs from one device to another device across Link.



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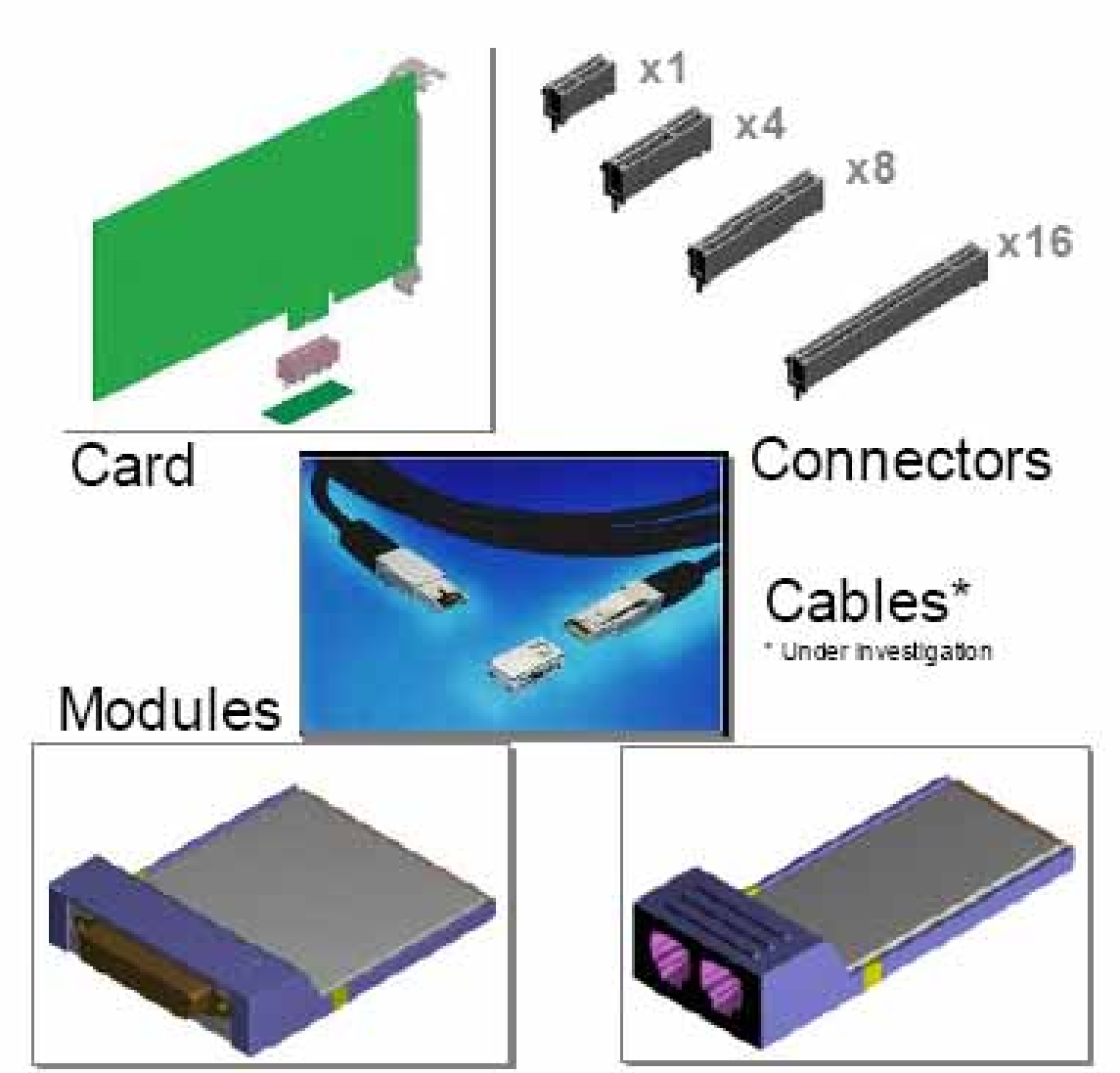
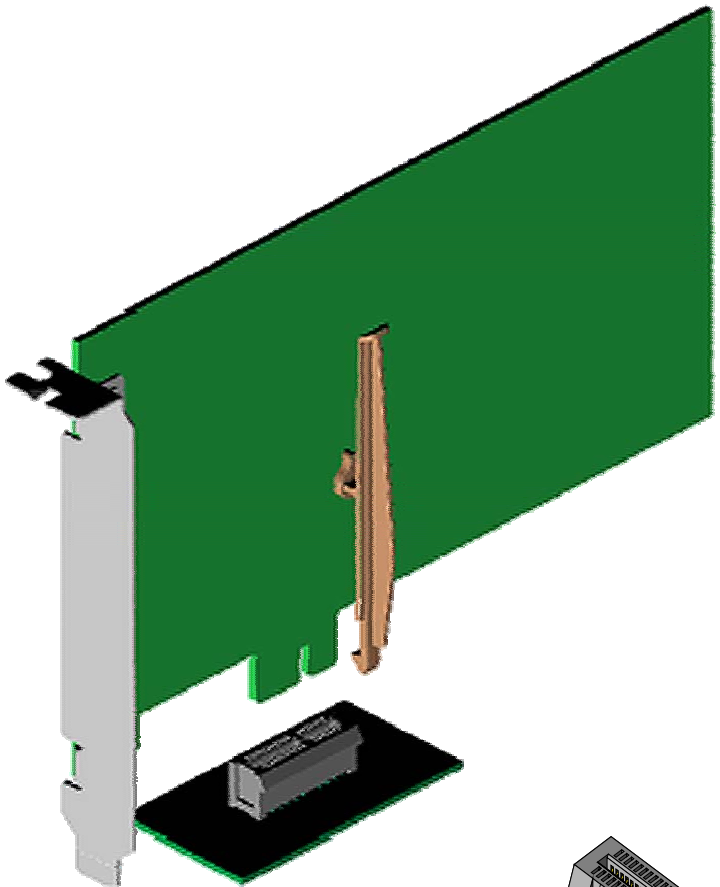
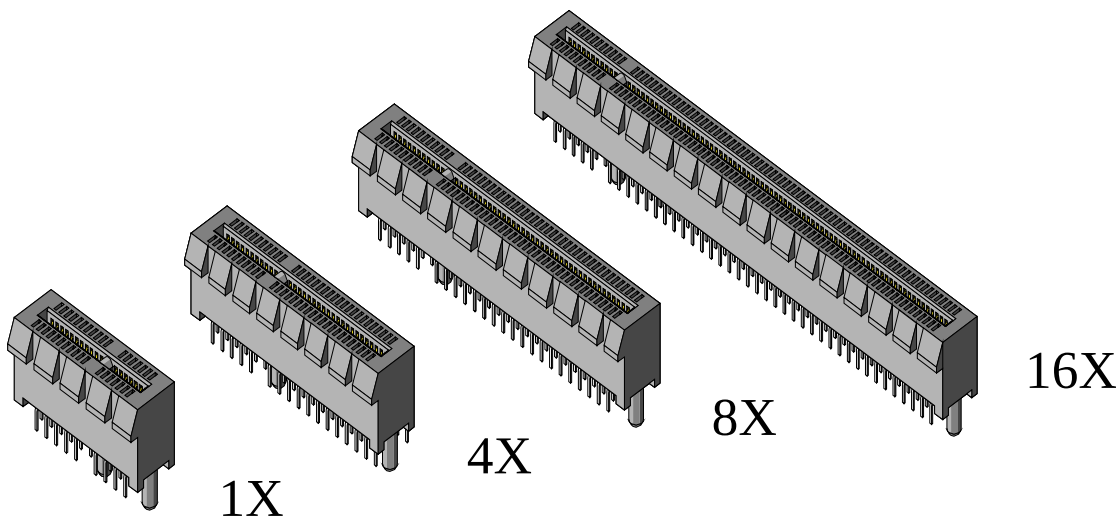
PCI Express Mechanicals



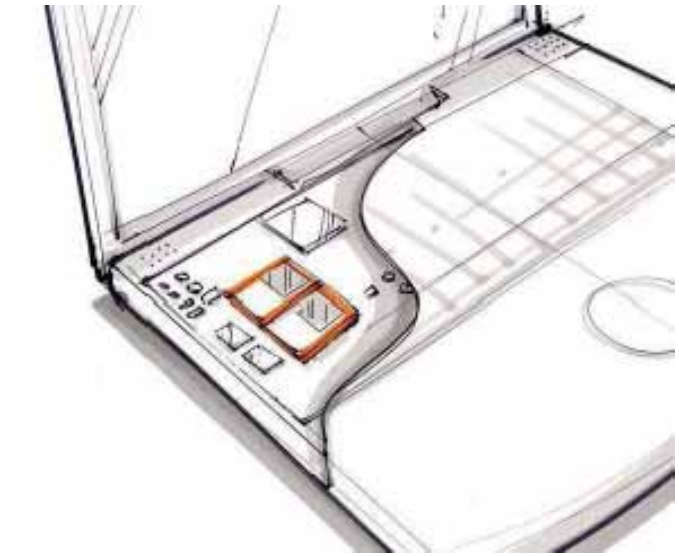
Desktop & Server Form Factor



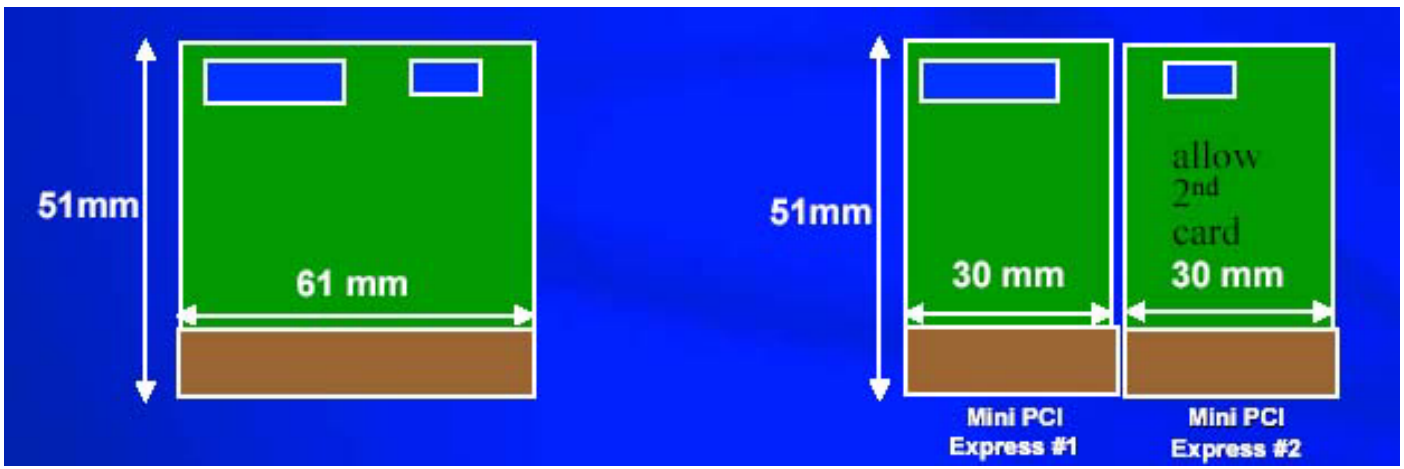
- Motherboard usage
- Supports I/O & graphics
- First available form factor
- Systems will ship in 1H04



MiniCard Form Factor



- Replacement for Mini-PCI
- Wired & wireless comm



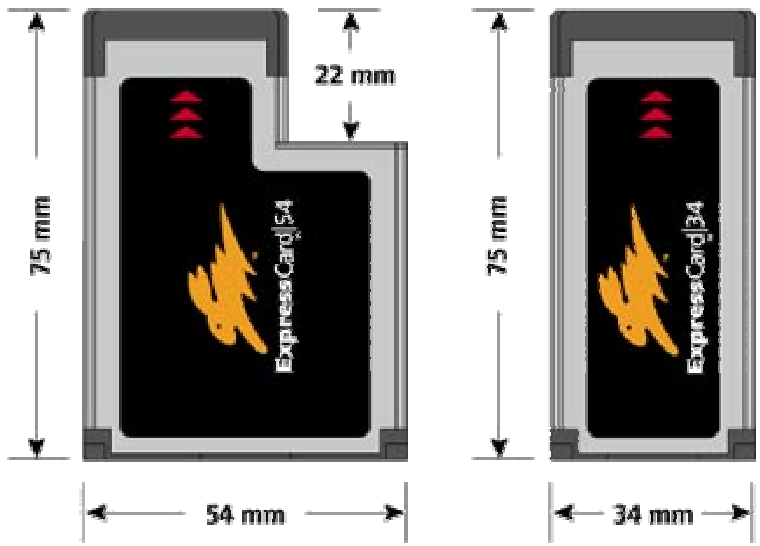
Current Mini-PCI Card

New Mini PCI Express Cards

ExpressCard Form Factor

- Replacement for CardBus
- Modular expansion
- Host will support PCI Express & USB 2.0
- For notebooks

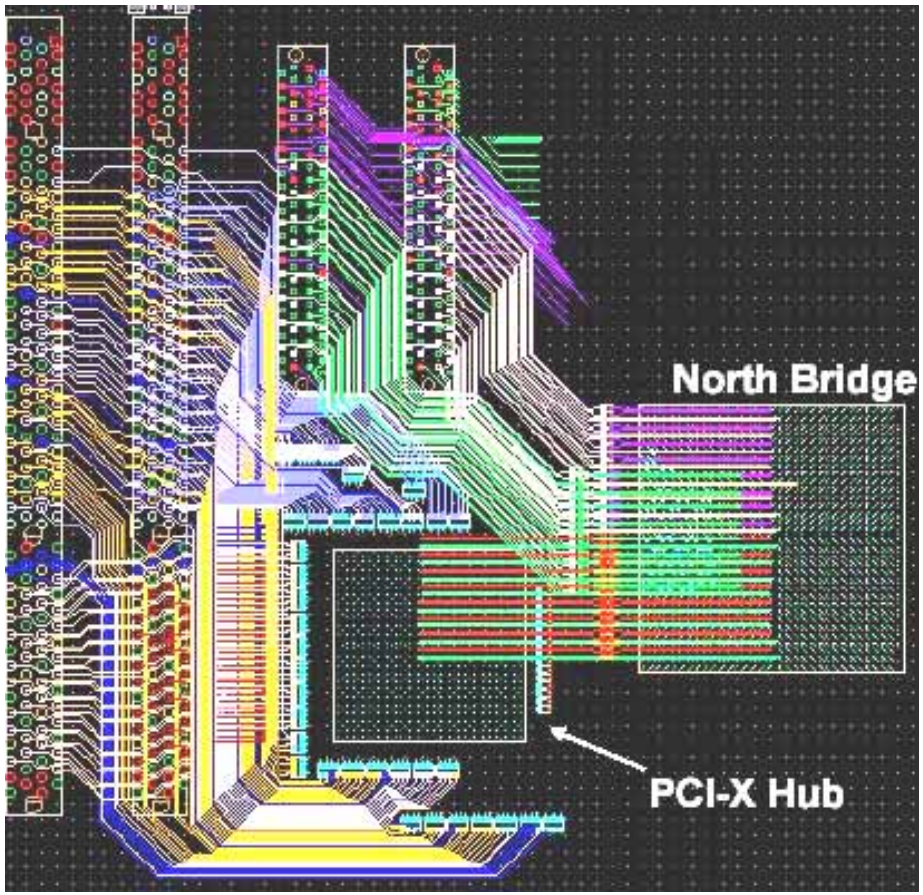
Current CardBus



New ExpressCard Types

Routing Advantages of PCI

PCI-X
64 Bit



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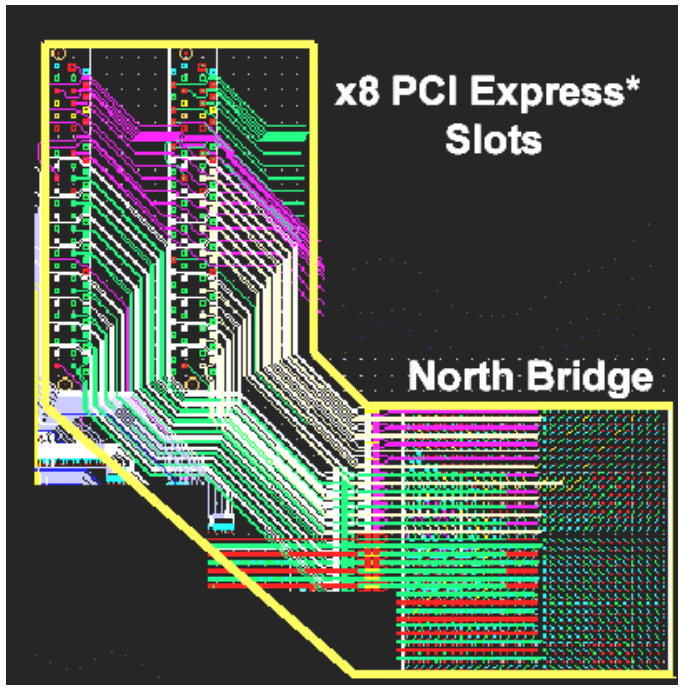
Routing Advantages of PCI Express



- Board area reduced by 53%
- Reduction of number of board layers