What is LDO (Low-Dropout Voltage Regulator)

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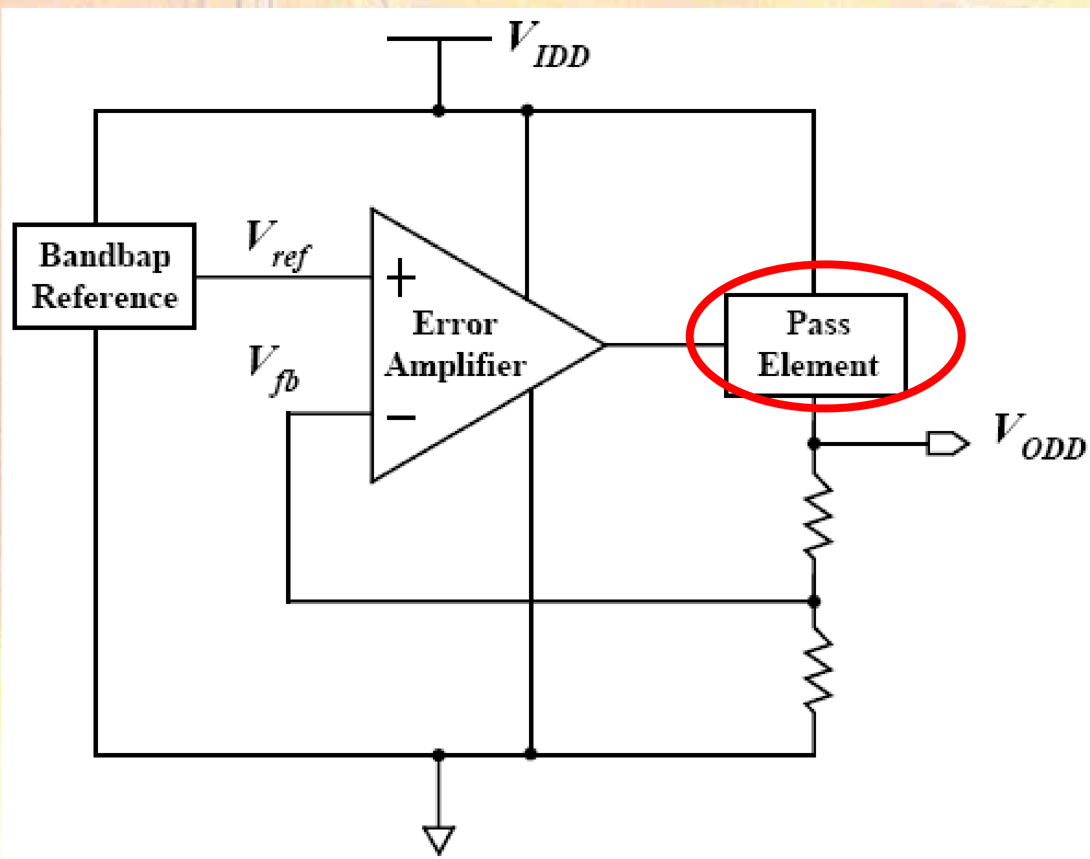
Agenda

- *What is LDO?*
- *Why use LDO?*
- *Major types of LDO*
- *How to select a LDO?*
- *Other design issue*

What is a LDO?



Basic LDO architecture

VIDD: Input voltage

VODD:Output voltage

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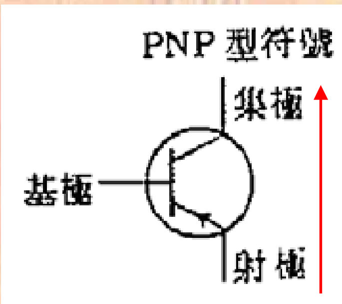
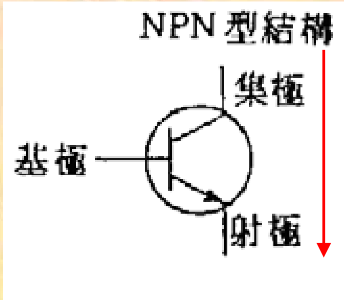
Pass elements of LDO

Transistor:

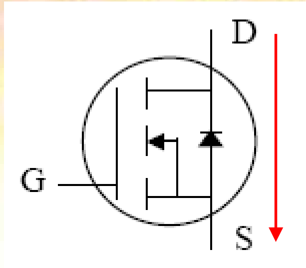
PNP **NPN**

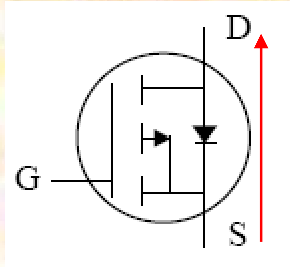




MOSFET:

N-MOS **P-MOS**





Transistor:

$I_c = \beta * I_b$

$I_c = \alpha * I_e$

$\alpha = \beta / (\beta + 1) < 1$

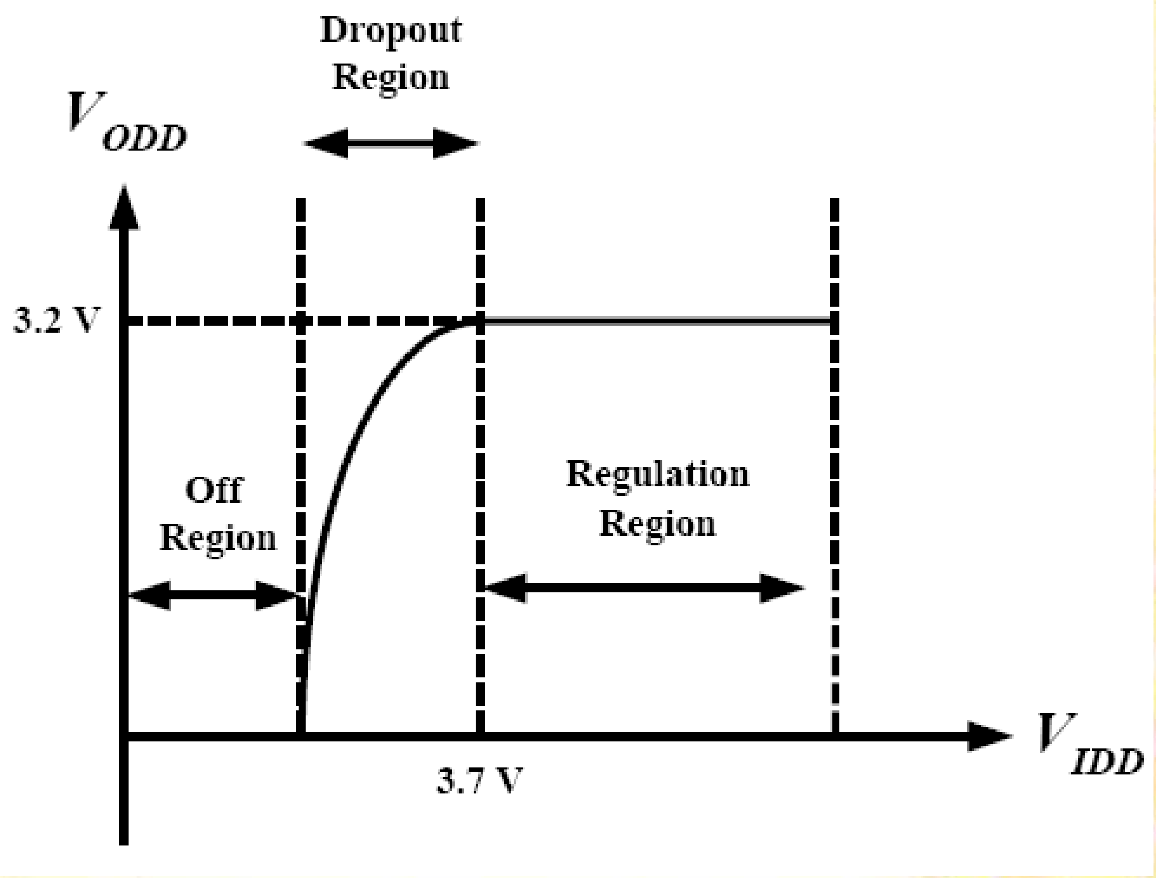
MOSFET:

Working on resistive region

$I_D = K[2(V_{GS} - V_T) V_{DS} - V_{DS}^2]$

V_T = threshold voltage

K= conductance parameter



LDO input and output voltage

Why Linear?

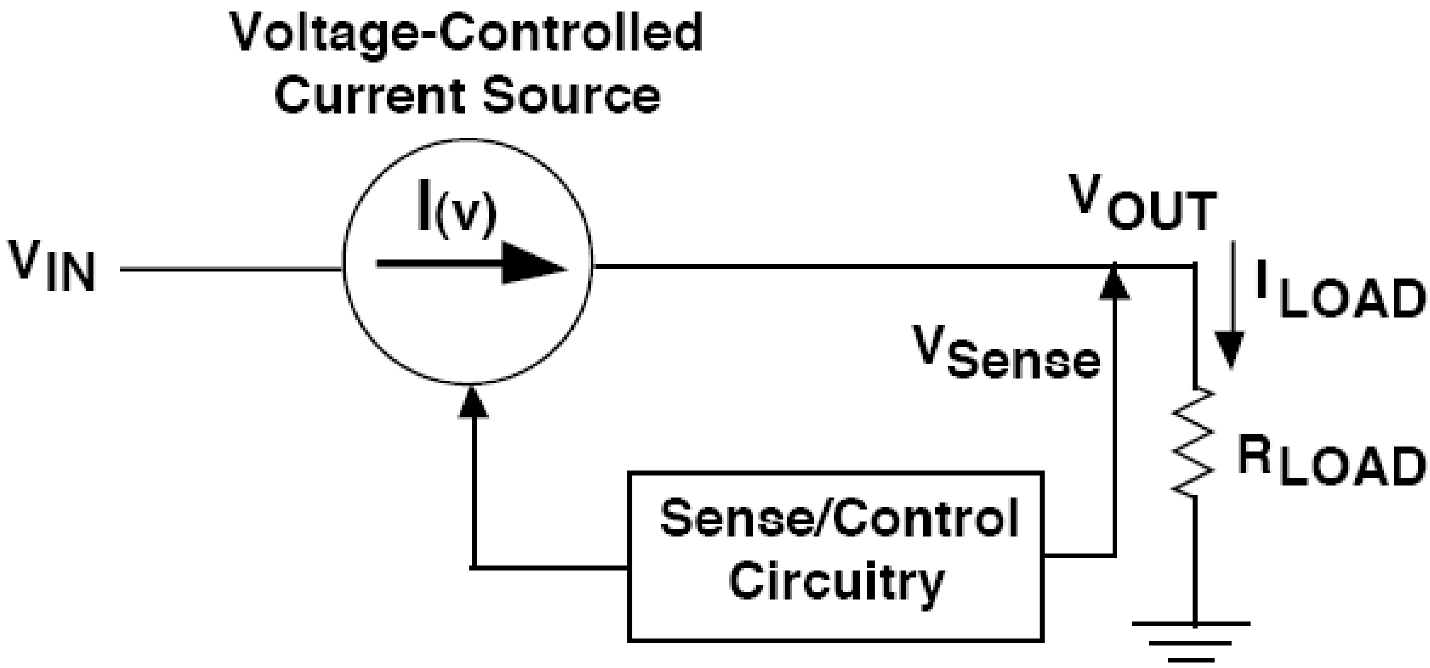
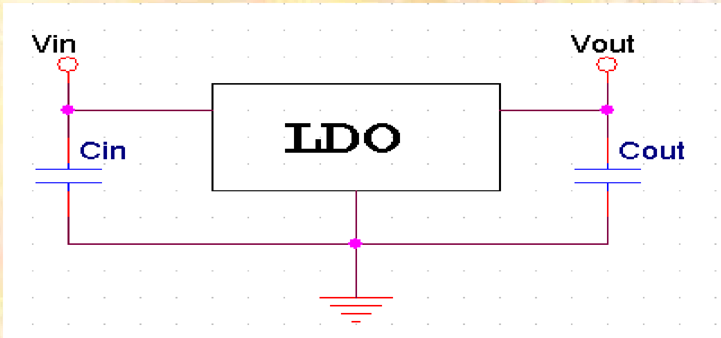


FIGURE 1. LINEAR REGULATOR FUNCTIONAL DIAGRAM

Why use LDO?



Benefits :

- ✓ Low cost & Easy-to-use
- ✓ Accurate supply voltage
- ✓ Active noise filtering
- ✓ Protection from over-current faults
- ✓ Generation of multiple output voltages from a Single source

Fault:

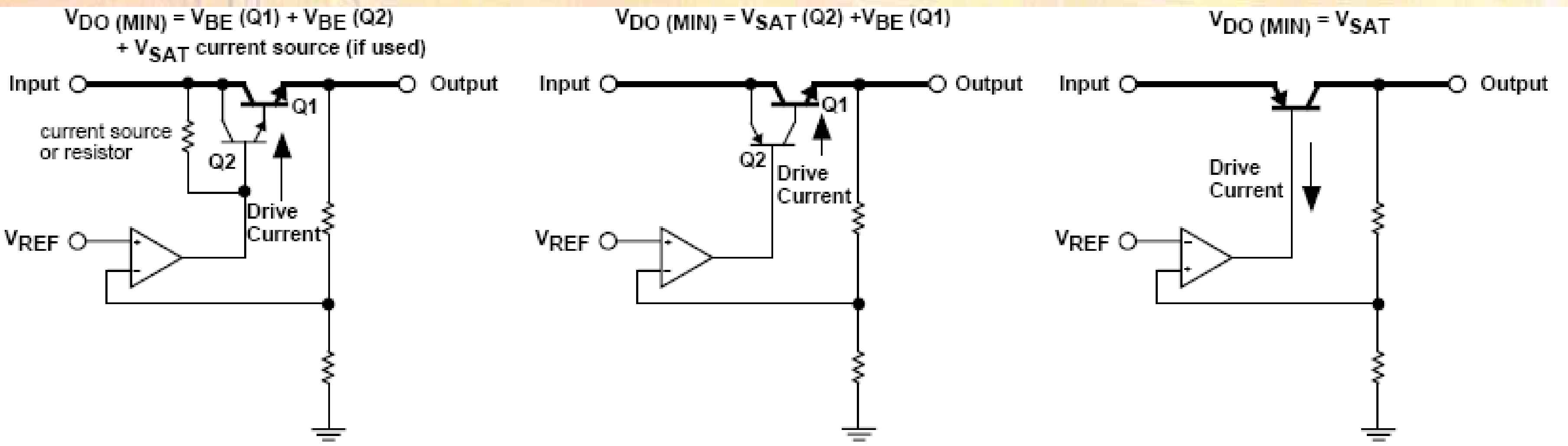
- ✓Efficiency is bed
- ✓Thermal issue

Why use LDO?

Who Prefers LDO?

- ✓ Communications equipment
- ✓ Small devices
- ✓ Battery operated systems
- ✓ Low current devices
- ✓ High performance microprocessors with sleep mode (fast transient recovery required)
- ✓ Analog Device (Audio power,RF power…)

Techmosa *Major types of LDO*



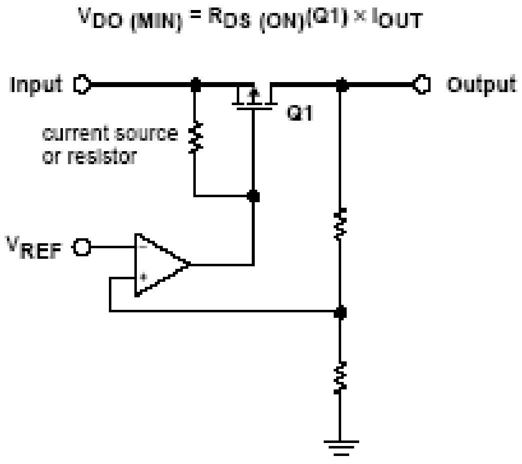
(A) Standard NPN-pass transistor regulator *(B) NPN-pass regulator with reduced dropout* *(C) Low-Dropout PNP-pass transistor regulator*

(A) "Classic" NPN-based regulators that require 2.5 to 3V of excess input voltage to function.7805,317,340

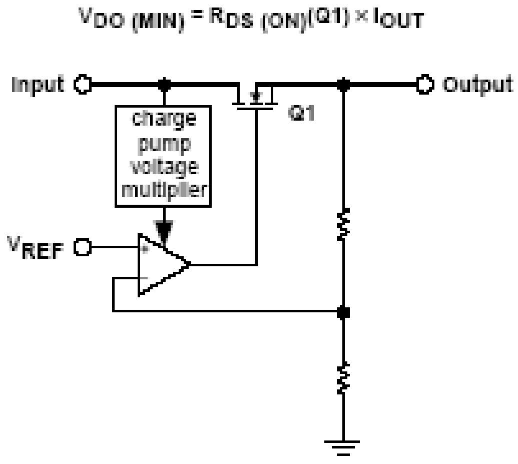
(B) "Low Dropout NPN" regulators, with a NPN output but a PNP base drive circuit. These devices reduce the dropout requirement to 1.2 to 1.5V.

(C) True low dropout PNP-based regulators that need 0.3V to 0.6V extra for operation.

Major types of LDO



(D) P-Channel MOSFET-pass transistor regulator



(E) N-Channel MOSFET-pass transistor regulator

(D) P-channel CMOS output regulators.

These devices have very low dropout voltages at low currents but require large die area (hence higher costly than bipolar versions)

(E) Regulator controllers.

Provide the control functions of a linear regulator, and do not have the pass element on it.

It provide the advantage of optimizing die area and cost for higher current applications.

Techmosa Major types of LDO

效能	Darlington	NPN	PNP	NMOS	PMOS
靜態電流	中等	中等	大	小	小
Dropout 電壓	$V_{EC(sat)}+2V_{BE}$	$V_{EC(sat)}+V_{BE}$	$V_{EC(sat)}$	$V_{SD(sat)}+V_{GS}$	$V_{SD(sat)}$
負載推動力	大	大	大	中等	中等
暫態反應速度	快	快	慢	中等	中等

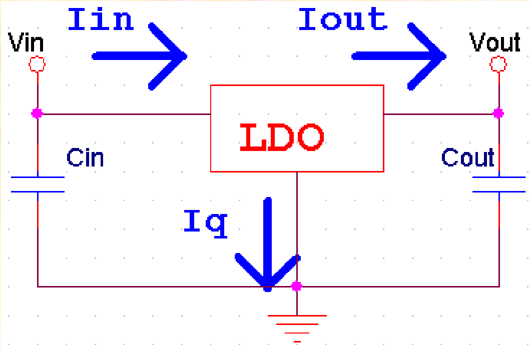
各種傳輸元件的效能比較

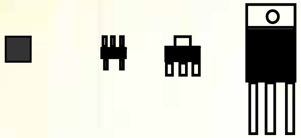
%各有優劣%

How to select LDO?

The most important parameters of LDO:

- Input voltage (Vin)
- Output voltage (Vout)
- Maximum output current (Iout)
- Dropout voltage
- Ground current /quiescent current (Iq)
- Power disspation = (Vin-Vout) *Iout +Vin* Iq
- Package



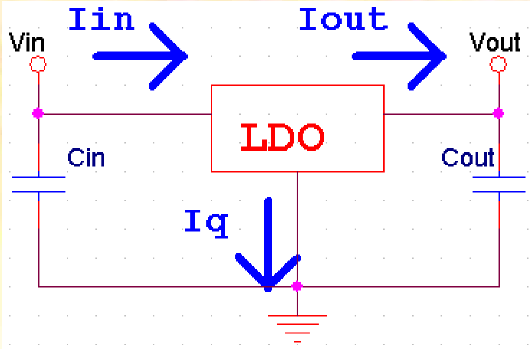


Other design issue

Component selection:

❑ ***Input capacitor***

- **Depends your Vin power quality.**
- **Larger values may be required if Vin has high ripple.**
- **X7R,X5R ceramic capacitor can be used for bypassing.**



❑ ***Output capacitor***

- **There is recommend minimum value of it.**
- **Compensation**
- **Low inductance, low ESR would be better.**
- **PNP&PMOS LDO need specified range ESR value.**
- **Exp: X7R,X5R,Tantalum**

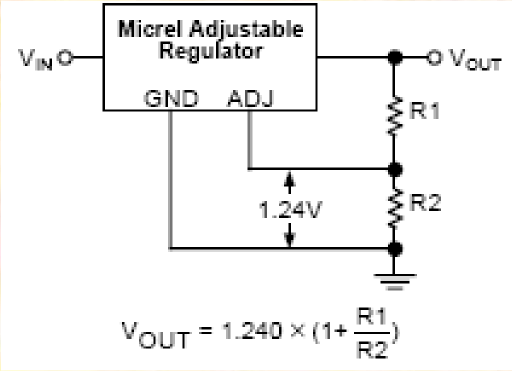
Techmosa *Other design issue*

❑ ***LDO Efficiency:***

Eff= Pout / Pin= Vout*Iout / Vin*Iin

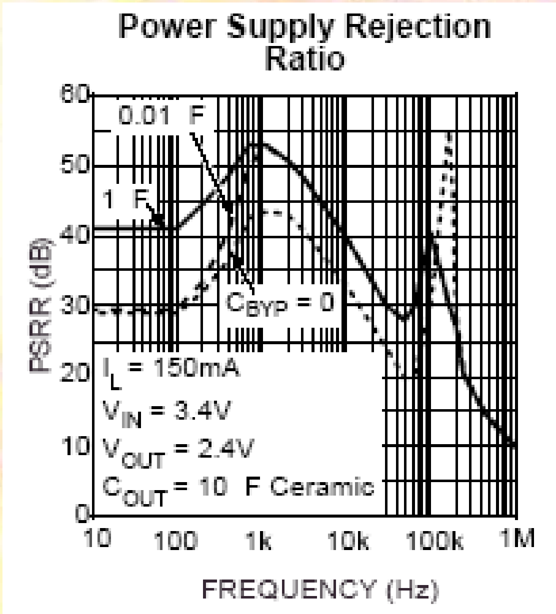
And , Iout ~= Iin

A close efficiency approximation : Eff = Vout / Vin



❑ ***Power Supply Rejection Ratio(PSRR):***

PSRR(dB)=20Log(△ Vin/ △ Vout)



Techmosa Other design issue

❑ *Thermal Management*

- LDO power dissipation and heat-sink requirements for various 3.3V current levels.

Regulator	I_{OUT}	P_D (W)	θ_{SA}(°C/W)
MIC29150	1.25A	2.6	25
MIC29150	1.5A	3.2	21
MIC29300	2.0A	4.2	15
MIC29300	2.5A	5.2	11

- **Θ Thermal resistance(C/W)**

  Θ =△T/Q

  △T: Temperature difference

  Q : Power dissipation

- **Θ SA : Haet Sink to Ambient (free air) Thermal resistance**

- Ambient Temperature Affects Heat Sink Requirements

Output	Ambient Temperature		
	40°C	50°C	60°C
1.5A	24°C/W	21°C/W	17°C/W
5A	5.1°C/W	4.1°C/W	3.2°C/W

Techmosa *Other design issue*

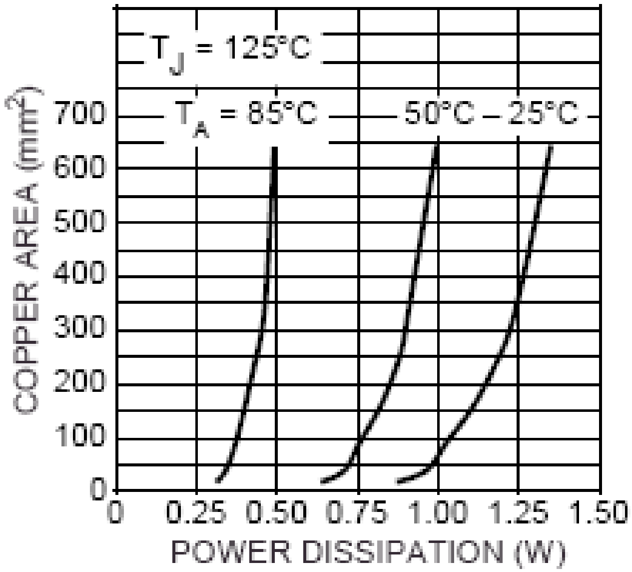


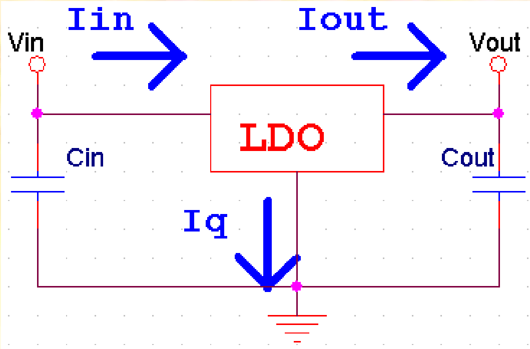
Figure 5. Copper Area vs. Power-SOIC Power Dissipation

The minimum amount of copper can be determined by knowing the maximum power dissipation required.

Techmosa Other design issue

What is a high performance LDO?

- ✓ Wide Vin voltage range
- ✓ Low Iq current
- ✓ Low dropout voltage
- ✓ Small output capacitor
- ✓ High PSRR
- ✓ Over current protection
- ✓ Fast Transient Response
- ✓ Low Thermal resistance
- ✓ Small package



Q&A

Thank You !